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## Application Series

### SunSet xDSL: IDSL Testing with an External Reference Clock

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## INTRODUCTION

IDSL stands for ISDN Digital Subscriber Line (IDSL). IDSL uses the same 2B1Q line encoding as ISDN Basic Rate (BRI) and operates up to 18,000 feet (5.5 km). Because IDSL uses the same industry-standard line coding technique as ISDN, customers with ISDN BRI terminal

adapters can use their current TAs, routers and bridges for connecting to IDSL lines. Any of the commonly used transport protocols such as PPP, MP, MP+ or Frame Relay may be used over the IDSL line allowing rapid and transparent integration into Internet, remote LAN access and telecommuting.

IDSL circuits are very often transported through carrier systems, e.g. Adtran U-BRiTE, etc., on which a number of IDSL circuits are multiplexed and transmitted over a distance before they are fanned out to individual customer premises. Figure 1 illustrates a typical IDSL system. Timing synchronization is a key element for this setup. The DSLAM co-located or at the central office receives timing from a T3 connection from the ATM network. The channel bank (U-BRiTE card) at the central office derives network timing from one of the U interface connections from the DSLAM. The remote channel bank is set for loop (receive) timing and retrieves its timing off the T1 signal coming from the central office U-BRiTE system. Thus, the signal remains synchronized from the ATM T3 all the way to the customer's NT1/TA equipment.

## TESTING IDSL CIRCUITS

A common turn-up test for IDSL circuits is to connect a test set at the central office replacing the DSLAM and

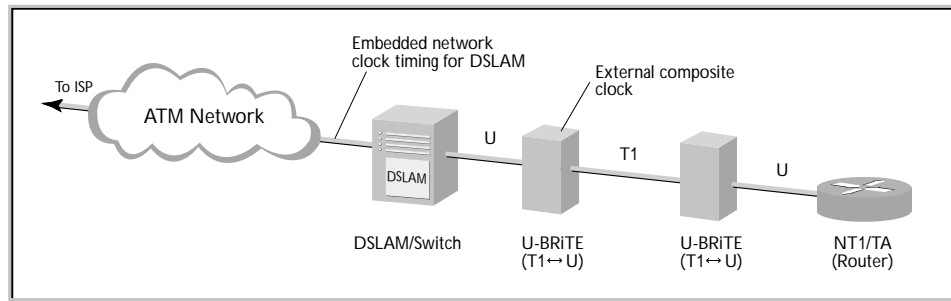


Figure 1 IDSL transported via channel bank

facing the customer. The other end of the circuit is either terminated by another test set or even Customer Premises Equipment (CPE) capable of responding to eoc loop back commands. A BERT test is then performed to qualify the circuit.

When testing those IDSL circuits transported over synchronous carrier systems as discussed above, the test set needs to be similarly synchronous to the network in order to provide accurate BERT results. If the test set is not properly synchronized, intermittent pattern loss and bit errors shall occur due to clock slips. **Therefore, it is critical to use an external clock source when testing these IDSL circuits.** The SunSet xDSL IDSL module provides two different external clock configurations.

### U External Clock

The U Ext. Clock enables the SunSet to derive timing from a U interface 2B1Q signal. This U-2B1Q reference signal can be obtained from the output of the IDSL interface of the DSLAM, which is normally connected to a network clock reference, e.g. via a T3 connection. This IDSL interface could be the original circuit provisioned or one dedicated for testing. Figure 2 depicts the use of such a U interface clock reference with the IDSL module.

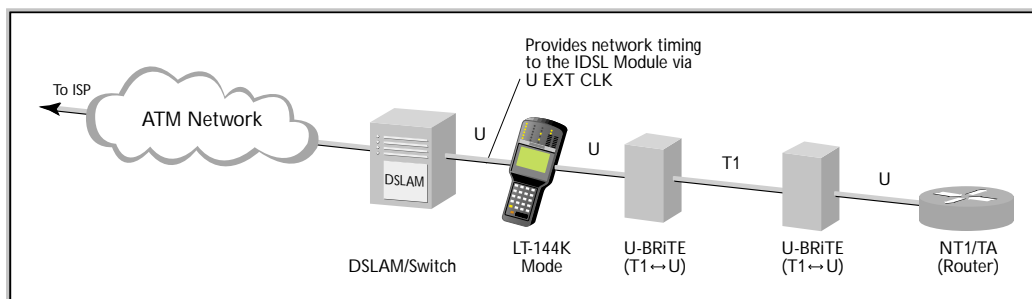


Figure 2 U EXT CLK: timed from the DSLAM U interface

### T1/E1 External Clock

The T1/E1 Ext. Clock input enables the retrieval of clock reference from a T1 or E1 signal. A T1 reference signal can be obtained from the output of an on-site reference clock or any T1 signal carrying the network clock reference. Figure 3 depicts this setup. Now the test set and the Channel Bank are synchronized to the same reference source and clock slips are thus eliminated when running BERT testing over the IDSL circuit.

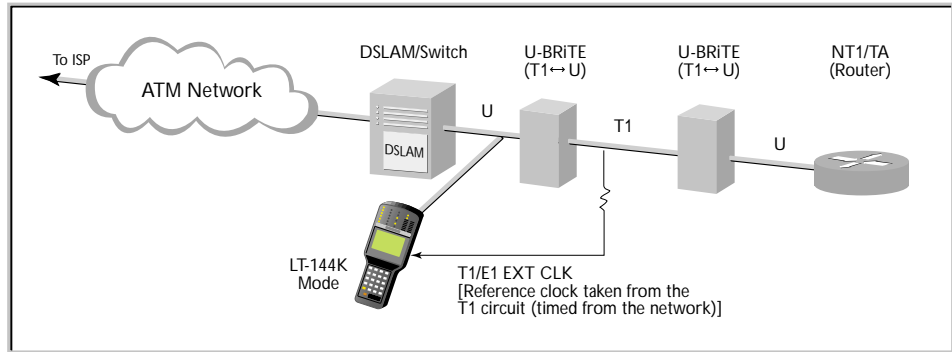


Figure 3 T1/E1 EXT CLK: timed from the T1 signal

### PERFORMING A BERT TEST FROM THE CENTRAL OFFICE

The following application outlines a simple turn-up procedure from the central office. This application uses the LT mode, where the SunSet xDSL emulates the switch (LT) located in the central office. This mode can be used to troubleshoot ISDN basic rate and IDSL circuits by looping U-BRiTE cards, U repeaters, or the NT1 device.

1. Press the MODULE key. The xDSL LED will light green indicating the set is in xDSL (here IDSL) mode.
2. Enter IDSL TEST for IDSL testing.
3. Enter TEST CONFIGURATION. Refer to Figure 4. Configure the screen as follows:  
INTERFACE: U  
MODE: LT-144K  
XMT CLK: EXT-U (or as applicable)  
TEST CHANNEL: 2B+D  
TEST PATTERN: 2047
4. Connect the set to the IDSL circuit. Connect the 2B1Q U interface span to the U-2B1Q jack on the module. If you have selected an external timing source, make sure to plug the timing reference into the appropriate jack. If you are using timing from the U interface, connect the IDSL output from the DSLAM or switch into the U EXT CLK jack on the module.
5. Notice the LEDs on the SunSet. The T1/E1 SIG LED should now be solid green, indicating you are receiving a signal at the U interface. The LP 1 SYNC shows the status of synchronization. This light should be solid green, indicating that the set has achieved Layer 1 frame sync. If the LP 1 SYNC LED is solid red, the set does not have frame sync.

```

MEAS 13:27:10

TEST CONFIGURATION

INTERFACE : U
MODE      : LT-144K
XMT CLK   : EXT-U
TEST CHANNEL: B1+B2
TEST PATTERN: 2047

U S/T

```

Figure 4 IDSL setup

6. Next, you can loopback an NT1 or repeater (U-BRiTE card) and run a BERT test. Escape from the Test Configuration screen.
7. Enter EOC CONTROL. Refer to Figure 5.
8. At ADDRESS, press the NEXT (F2) key until the address at the right displays the equipment you want to loop back. First, you should loop up the NT1 device to test the whole 2B1Q span. If you see errors, then you can try looping each U repeater/U-BRiTE card on the span to sectionalize the problem. To loop up the NT1, make sure ADDRESS reads 0 (NT1).

```

MEAS 12:00:27

EOC CONTROL

RX ADDRESS : 0 (NT1)
COMMAND    : B1 LOOPBACK
EOC BITS   : 000101010001
-----
RX ADDRESS : 7 (GLOBAL)
RX COMMAND : B1 LOOPBACK
RX EOC BITS: 000101010001

SEND LOOPB1 LOOPB2 more

```

Figure 5 EOC control

9. At COMMAND, select the message to send. To loopback the full 2B+D (144k) pipe, select LOOP2BD (F3). After selecting the proper message, press SEND (F1).
10. Watch the receive command at the bottom of the screen (RX COMMAND). When the repeater loops up, you should see your message return to you. If you never see the Loop up message return, the device has not successfully looped up.
11. After looping the device, you can run a BERT test to check for bit errors. Escape from the EOC CONTROL screen.
12. Enter BERT & RESULTS. The PAT SYNC LED should be solid green, indicating that the set has achieved pattern synchronization. If the test runs clean and there are no errors, you have just verified the entire 2B1Q span. If the set is taking bit errors, you should return to the EOC CONTROL and try looping each U repeater on the span to sectionalize the fault.
13. When you have finished testing the NT1, you must loop it down and normalize the span.



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