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## Application Series

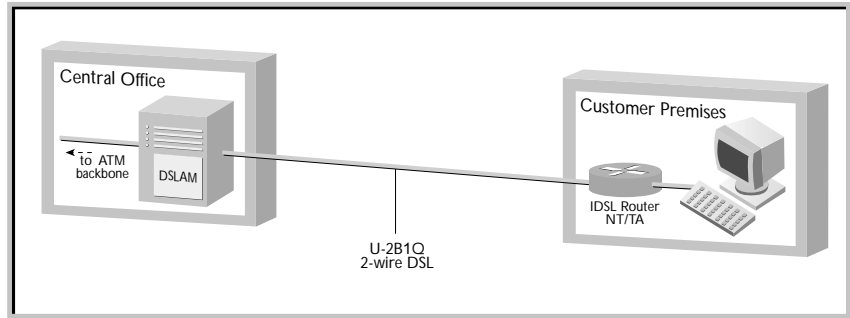
### SunSet xDSL IDSL Module: IDSL Circuit Testing

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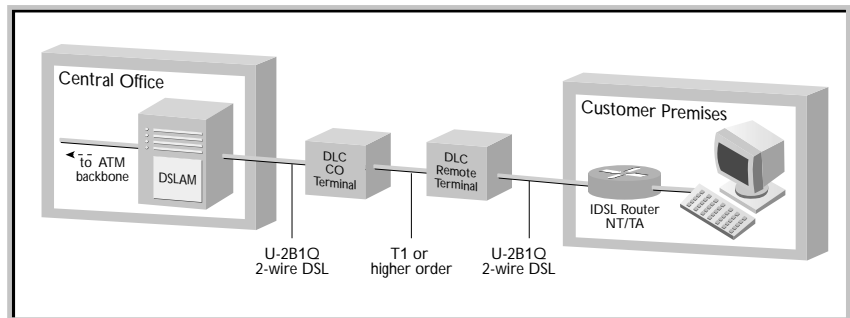
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## TRANSPORT FOR IDSL CIRCUITS

IDSL Circuits can be provisioned from the DSLAM at the Central Office (CO) location to the Customer Premises Equipment (CPE) over a copper pair directly (as shown in Figure 1), if the customer is located within the reach range (about 18,000 feet without repeaters). A number of IDSL circuits can also be multiplexed and transported over a Digital Loop Carrier (DLC) system, which meets the Telcordia TR-TSY-000397 requirement to bring IDSL service to a cluster of customers in the same area (refer to Figure 2).



**Figure 1 IDSL Circuit transported over a 2-wire Copper Pair**



**Figure 2 IDSL Circuit transported over a Digital Loop Carrier**

## TESTING IDSL CIRCUITS

The turn-up of an IDSL circuit requires verifying end-to-end continuity and bit error performance of the circuit between the CO and the CP. There are two possible ways to achieve the verification test for the circuit:

- Single-ended test: Only one test set is required and the circuit can be tested from either:
  - The central office where the test set emulates the Line Termination (LT) device, i.e. the DSLAM or,
  - From the field where the test set emulates the customer premises equipment (NT).
- Two-ended test: Two test sets are required, one emulates the LT at the CO location and the other emulates the NT at the CPE location.

## SINGLE-ENDED TESTING FROM THE CENTRAL OFFICE

In general, single-ended testing is done from the CO location. A test set, emulating the LT at the CO, is connected to the IDSL circuit under test. Then, ANSI T1.601 embedded operations channel (eoc) loop up commands can be sent to loop up the IDSL Router (NT/TA) at the CP if it has been installed. A Bit Error Rate Test (BERT) can then be run towards the loop, to verify the performance of the circuit.

For an IDSL circuit transported over a DLC system, it is required that the DLC be configured to use the 3-DSO TDM multiplexing method to enable eoc commands to pass through the system. In this method, the DLC designates three DSO channels to transport the entire 2B+D payload plus the overhead from one end to the other end of the system. This method also enables eoc loop commands to be sent to the channel unit cards (U-BRiTE cards), which act as repeaters at either the DLC CO Terminal or the DLC Remote Terminal. These loop commands can help when troubleshooting the line cards. If the DLC is set to run in Transparent mode, the eoc channel will not be passed through the DLC to the CPE and the loop commands will not be supported in the DLC system. Therefore, a two-ended test must be performed.

To successfully BERT test an IDSL circuit over a DLC, the test set must be synchronized to the network clock to avoid intermittent pattern sync loss due to clock slips. This is detailed in the SunSet xDSL Application Series, Publication Number APP-XDSL-010, IDSL Testing with an External Reference Clock.

The single-ended tests from the CO (Figures 3 and 4) are applicable only if the CPE has already been connected to the IDSL circuit, or if the DLC system supports and passes through the eoc channel. If the eoc is supported, the SunSet xDSL with an IDSL Module will be able to loopback not only the CPE, but also the channel unit line cards in each of the DLC Terminals (CO and Remote) for BERT analysis.

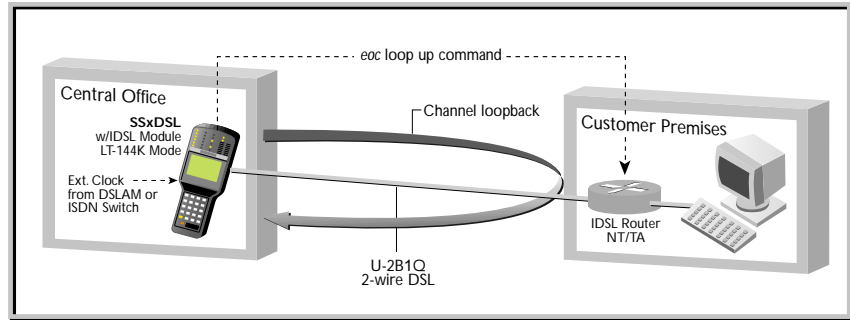


Figure 3 Single-ended test on IDSL Circuit from the CO

### Configuring the Test Set

The configuration of the test set is similar for testing an IDSL circuit over a copper pair or over a DLC system. The only difference is the TX CLOCK setting. For testing IDSL over a copper pair, the TX CLOCK source should be set to INTERN, to use the internal clock of the test set. However, for IDSL circuits carried over a DLC, an external reference clock should be used to synchronize the test set to the network. In most cases, a U interface signal from either the DSLAM or an ISDN switch is used, so TX CLOCK should be set to EXT-U (as shown in Figure 5).

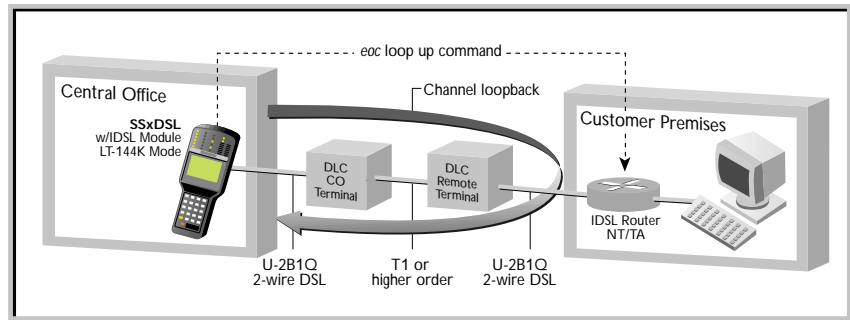


Figure 4 Single-ended test on IDSL Circuit transported over a DLC from the CO

The TX CLOCK setting is only available when the test set is configured to LT-144k. In this mode, the selected test pattern is sent in the test channel specified. As you cursor down to the TX CLOCK field, four F-keys will be displayed. Select the appropriate clock setting that fits the application to be run.

Connect the U-2B1Q connector of the test set to the IDSL circuit under test and connect the U EXT CLK connector to the external clock source, if applicable. The TEST CHANNEL selection should be set to 2B+D to BERT test the IDSL circuit at the full rate of 144 kbps. You can also select a smaller set of channels to BERT test at a lower speed.

The T1/E1 SIG LED should turn green, followed by the LP1 SYNC LED after Layer 1 frame synchronization is acquired. When the TX CLOCK field is set to EXT-U, the FRAME LED will be used to indicate the status of the external clock input. The FRAME LED will be solid green to indicate a proper external clock signal, or will be red if the external clock is not received properly.

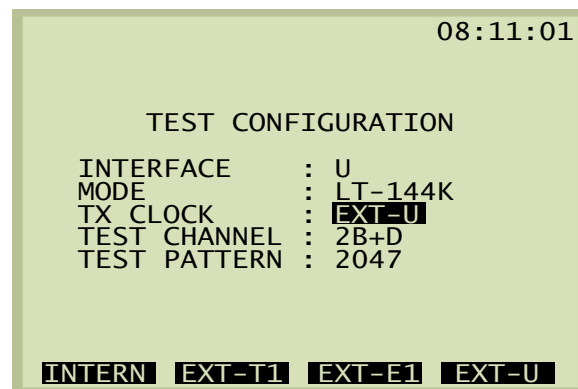


Figure 5 IDSL Module TEST CONFIGURATION Screen

## Looping Up a Channel Unit Line Card or CPE

Escape from the TEST CONFIGURATION screen and enter the EOC CONTROL screen (Figure 6).

To loopback the IDSL Router (NT/TA), set the ADDRESS to 0 (NT1) and the COMMAND to LOOP2BD. This eoc command will then be sent to the NT (CPE) and will initiate a loopback of the B1, B2, and D-channels. Press the SEND F-key to transmit the eoc command. Check in the bottom half of the screen to see the RX (received) ADDRESS and COMMAND returned from the device. The RX ADDRESS and COMMAND should be identical to those transmitted. This indicates a successful command and response, and that the loopback is in place. If the identical message is not shown in the Received field, the loop command has failed.

## Running a BERT Test

Once the loopback is confirmed, a BERT test can be started. Escape from the EOC CONTROL screen and enter the BERT & RESULTS screen from the IDSL/ISDN BERT menu. Check that the PAT SYNC LED is solid green (indicating test pattern synchronization) and that the BIT ERR LED is off. Inject a bit error from the test set by pressing the ERR INJ key on the keypad. The BIT ERR LED should turn red for about one second and start blinking red. Check that the ERROR COUNT reads one; this verifies that the channel is properly looped back. Press the HISTORY key to acknowledge the error condition. You will notice that the BIT ERR LED will stop blinking. Press the STOP/START F-key twice to restart the BERT test. This will set the ERROR COUNT back to 0 (see Figure 7).

For testing a bit rate of 144 kbps (i.e. TEST CHANNEL setting of 2B+D), it is recommended by the ANSI T1.601 specification, that the BERT test be run for at least 10 minutes. For testing a bit rate of 64 kbps (i.e. TEST CHANNEL setting of B1 or B2), the test should be run for 25 minutes.

## SINGLE-ENDED TESTING FROM THE FIELD

The test set functions as an NT emulating the CPE, and the DSLAM is required to provide a loopback on the IDSL circuit to be able to perform a BERT test from the CP (Refer to Figures 8 and 9).

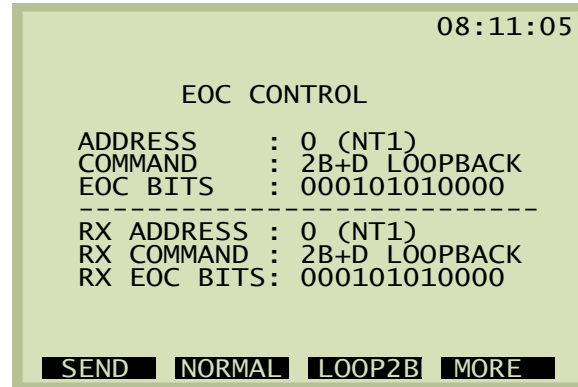


Figure 6 EOC CONTROL Screen

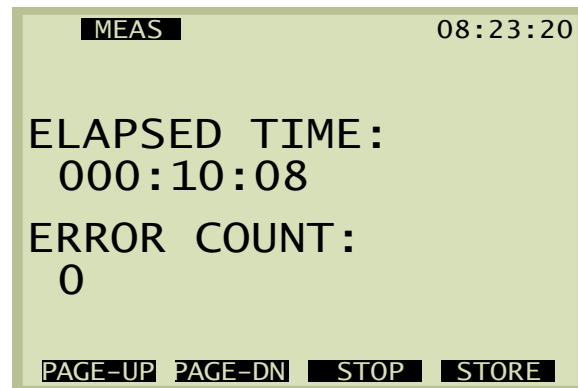


Figure 7 BERT & RESULTS Screen

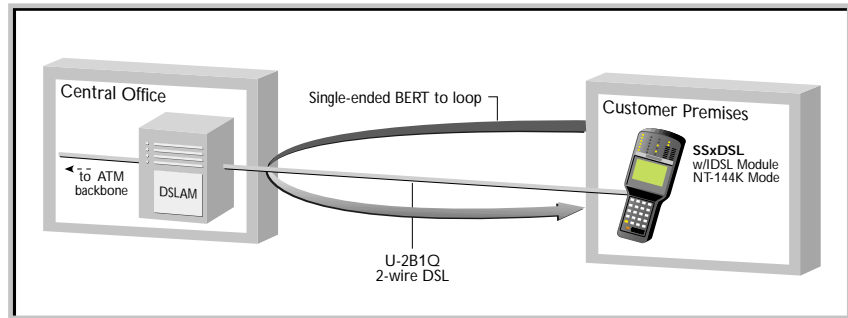


Figure 8 Single-ended test on IDSL Circuit from the CP

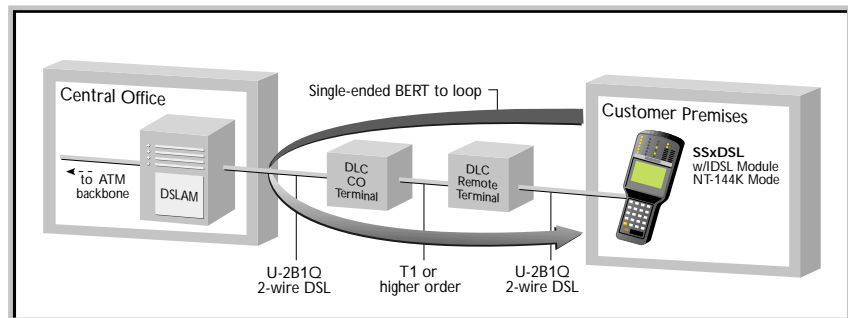


Figure 9 Single-ended test over a DLC from the CP

With the SunSet xDSL test set, you can choose which channels to run a BERT test on, from only the D-channel (16 kbps) to the full combined 2B+D channels (144 kbps).

If the eoc channel is not passed through the DLC system, or a loop cannot be placed at the DSLAM, a two-ended test is required to run a BERT test on the IDSL circuit.

### Configuring the Test Set

The configuration of the test set is identical for testing IDSL circuits over a copper pair or over a DLC. The configuration is as shown in Figure 10. The test set is configured to the NT-144k emulation mode and allows the user to configure a TEST PATTERN and designate which TEST CHANNEL is used.

Connect the U-2B1Q connector of the test set to the IDSL circuit under test. The TEST CHANNEL selection should be set to 2B+D to run the BERT test at the full rate of 144 kbps. As with single-ended testing from the CO, you can also select a smaller set of channels to BERT test at a lower speed.

The T1/E1 SIG LED should turn green, followed by the LP1 SYNC LED after Layer 1 synchronization is acquired.

### Checking Continuity to the DSLAM

If the IDSL goes through a DLC, a green T1/E1 SIG LED means that the test set has achieved Layer 1 frame synchronization to the last channel unit line card of the DLC. This does not necessarily mean you have connectivity all the way to the DSLAM. To confirm this, check the status of the ACT bit in the M4 channel, which is part of the overhead. Enter the M4 ACCESS screen (Figure 11). In NT-144k mode, the test set shows only the received M4 bits. The left most M4 bit displayed on the screen is the ACT bit. If it is set to a 1, or if the ACT indication is marked with an asterisk (\*), the circuit is connected through the DLC all the way to the DSLAM.

### Running a BERT Test

If a loop can be provided at the DSLAM, then a BERT test can be started on the IDSL circuit. Enter the BERT & RESULTS screen to start the BERT test. Check that the PAT SYNC LED is solid green (indicating test pattern synchronization) and that the BIT ERR LED is off. Inject a bit error from the test set by pressing the ERR INJ key on the keypad. The BIT ERR LED should turn red for about one second and start blinking red. Check that the ERROR COUNT reads one. This verifies that the channel is properly looped back. Press the HISTORY key to acknowledge the error condition. You will notice that the BIT ERR LED will stop blinking. Press the STOP/START F-key twice to restart the BERT test. This will set the ERROR COUNT back to 0.

```

09:11:01
-Power

TEST CONFIGURATION

INTERFACE      : U
MODE           : NT-144K
TEST CHANNEL   : 2B+D
TEST PATTERN   : 2047

NT-144K  LT-144K  NT-LOOP  LT-LOOP

```

Figure 10 TEST CONFIGURATION Screen

```

08:11:05
-Power

M4 ACCESS

NET → NT
M4  : 11111111
*ACT *DEA *SOC *UOA *AIB

```

Figure 11 M4 ACCESS Screen

## TWO-ENDED TEST OVER AN IDSL CIRCUIT

In this case, two test sets are used to test from each end of the IDSL circuit. One in the CO, emulating the LT (or the DSLAM), and the other at the customer premises emulating the NT (or the CPE). This test is extremely useful to qualify the cable pair and/or path provisioned by the DLC for IDSL service before the DSLAM is connected to the circuit and the CPE is installed. Because of the two-ended, bidirectional BERT test performed in this application, it will also detect directional problems from passing data over the IDSL circuit and through the DLC system.

### Configuring the Test Set

In this two-ended testing application, two SunSet xDSL units with IDSL modules are required (one at each end of the IDSL circuit - see Figures 12 and 13 on next page). The test set on the CO side of the circuit will be configured to LT-144k mode and the test set on the customer side of the circuit will be configured to NT-144k. Each test set should have the TEST CHANNEL set

to 2B+D in order to run the test at the full rate of 144 kbps. An external clock reference input for the LT-144k unit on the CO side of the circuit, is required if the circuit goes through a DLC system.

The configuration of the test set emulating the LT-144k mode is the same as that shown in Figure 5. The TX CLOCK is set according to the requirement as detailed in the Single-Ended Testing section. Refer to Figure 10 for the configuration of the test set emulating the NT-144k mode.

The T1/E1 SIG LED should turn green, followed by the LP1 SYNC LED after Layer 1 frame synchronization is acquired. If the circuit goes through a DLC, enter the M4 ACCESS screen on the NT-144k unit to confirm path continuity between the two test sets. This will allow you to observe the status of the ACT bit (see Figure 11). If it is set to a 1, or if the ACT indication is marked with an asterisk (\*), the circuit is connected through the DLC to the DSLAM, or in this case, the SunSet xDSL emulating the DSLAM (LT-144k). When set to 1, the end-to-end BERT test can be started by going to the BERT & RESULTS screen. Check that the PAT SYNC LED is solid green (indicating test pattern synchronization) and that the BIT ERR LED is off on both test sets. Inject a bit error from each of the test sets by pressing the ERR INJ key on the keypad. The BIT ERR LED should turn red for about one second and start blinking red. Check that the ERROR COUNT reads one. This verifies that the channel is properly looped back. Press the HISTORY key to acknowledge the error condition. You will notice that the BIT ERR LED will stop blinking. Press the STOP/START F-key twice to restart the BERT test. This will set the ERROR COUNT back to 0 (refer back to Figure 7).

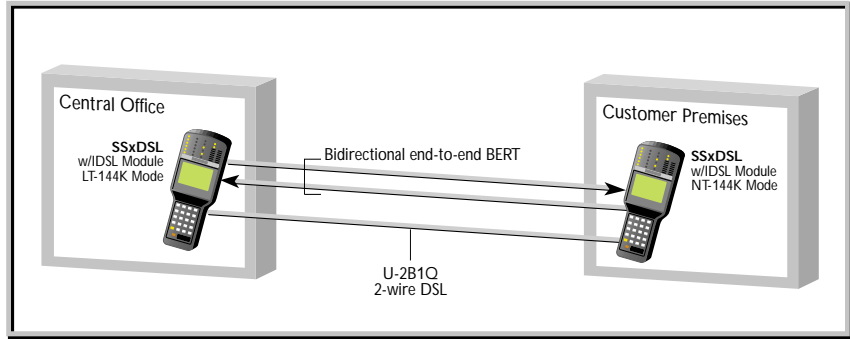


Figure 12 Two-ended test on an IDSL Circuit

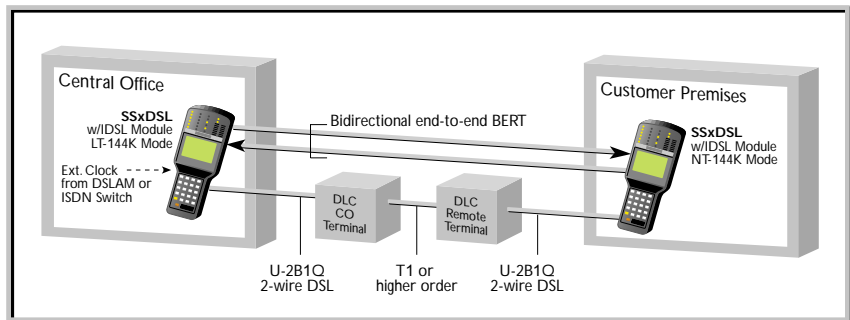


Figure 13 Two-ended test on an IDSL Circuit over a DLC